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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,933	08/13/2004	Jui-Hsiang Pan	11537-US-PA	4932

31561 7590 01/25/2007
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,933	PAN ET AL.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,16-18 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,16-18 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/15/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,303,978 Daniels et al.

1. Referring to claim 1, Daniels et al. teaches of a quad flat no-lead package structure, (the preamble does not provide significant patentable weight to the claims. See MPEP 2111.02.), comprising: a chip carrier, (Figure 1 #112), having a top surface and a bottom surface, wherein a plurality of conductive leads, (Figure 1 #113), is inlaid in the chip carrier, (Figure 1 #112), and lower surfaces of the conductive leads are exposed by the bottom surface of the chip carrier, (Figure 1 #112), while a plurality of pads, (Figure 1 the pad that #130 is attached to), is disposed on the top surface of the chip carrier, (Figure 1 #112), the conductive leads, (Figure 1 #113), being electrically connected to the pads, (Figure 1 the pad that #130 is attached to); and at least a chip, (Figure 1 #121), disposed on the top surface of the chip carrier, (Figure 1 #112), and electrically connected, (Figure 1 #130), to the chip carrier, (Figure 1 #112).

2. Referring to claim 2, Daniels et al. teaches of a package structure as claimed in claim 1, further comprising a passivation layer, (Figure 1 #142), to cover the chip, (Figure 1 #121).

3. Referring to claim 3, Daniels et al. teaches of a package structure as claimed in claim 1, wherein the chip carrier, (Figure 1 #112), includes an interconnect layer, (Figure 1 the area

between #113 and the pad in the top surface of #111), between the pads, (Figure 1 the pad that #130 is attached to), and the conductive leads, (Figure 1 #113), and wherein the interconnect layer, (Figure 1 the area between #113 and the pad in the top surface of #111), includes at least a via, (Figure 1 the area between #113 and the pad in the top surface of #111), for connecting one of the pads, (Figure 1 the pad that #130 is attached to), and one of the conductive leads, (Figure 1 #113).

4. Referring to claim 6, Daniels et al. teaches of a package structure as claimed in claim 1, wherein the chip, (Figure 1 #121), is electrically connected to the chip carrier, (Figure 1 #112), through surface mount technology, (Figure 1 #150).

5. Referring to claim 7, Daniels et al. teaches of a package structure as claimed in claim 6, wherein an anisotropic conductive paste, (Figure 1 #150), is further included to attach the chip, (Figure 1 #121), and the chip carrier, (Figure 1 #112).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, & 7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,911,736 Nagarajan.

6. Referring to claim 1, Nagarajan teaches of a quad flat no-lead package structure, (the preamble does not provide significant patentable weight to the claims. See MPEP 2111.02.),

comprising: a chip carrier, (Figure 1 #16), having a top surface and a bottom surface, wherein a plurality of conductive leads, (Figure 1 #26), is inlaid in the chip carrier, (Figure 1 #116), and lower surfaces of the conductive leads, (Figure 1 #26), are exposed by the bottom surface of the chip carrier, (Figure 1 #16), while a plurality of pads, (Figure 1 #22), is disposed on the top surface of the chip carrier, (Figure 1 #16), the conductive leads, (Figure 1 #26), being electrically connected, (Figure 1 #24), to the pads, (Figure 1 #22); and at least a chip, (Figure 1 #12), disposed on the top surface of the chip carrier, (Figure 1 #16), and electrically connected, (Figure 1 #14), to the chip carrier, (Figure 1 #16).

7. Referring to claim 3, Nagarajan teaches of a package structure as claimed in claim 1, wherein the chip carrier, (Figure 1 #16), includes an interconnect layer, (Figure 1 24), between the pads, (Figure 1 #22), and the conductive leads, (Figure 1 #26), and wherein the interconnect layer, (Figure 1 #24), includes at least a via, (Figure 1 the area of #24), for connecting one of the pads, (Figure 1 #22), and one of the conductive leads, (Figure 1 #26).

8. Referring to claim 27, Nagarajan teaches of a package structure as claimed in claim 1, wherein all the pads, (Figure 1 #22), are covered by at least the chip, (Figure 1 #12).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,793,105 Pace.

9. Referring to claim 16, Pace teaches of a wafer-level package structure, comprising: a silicon wafer, (Figure 5a-h #510 and Col. 7 Lines 1-7), having a plurality of sections, (the terminology of a plurality of sections in a silicon wafer is being interpretated in the broadest reasonable sense because the claim does not recite any limitation that would limit it from the definition of the sections being sectioned into the left half of the chip and the right half of the chip, where Figures 5a-h shows two sections of a chip making an entire chip); a plurality of conductive blocks, (Figure 5a-h #520 and 521 is clearly in the shape of a block by simple geometry, hence the examiner is taking the broadest reasonable interpretation of the term block and where the claims and disclosure do not provide a scale where to base a narrower definition of a block), disposed on the silicon wafer, (Figure 5a-h #510), and in each of the sections of the silicon wafer, (Figure 5a-h #510); a metal interconnect layer, (Figure 5a-h #518), connecting the plurality of the conductive blocks, (Figure 5a-h #520 and 521), wherein the metal interconnect layer, (Figure 5a-h #518), comprises at least a via hole, (Figure 5a-h #517), and a plurality of pads, (Figure 5a-h #519), wherein the via hole, (Figure 5a-h #517), electrically connects one of the conductive blocks, (Figure 1 #121 or 122), and one of the pads, (Figure 5a-h #519), and wherein the pads, (Figure 5a-h #519), are disposed on an uppermost surface of the metal interconnect layer, (Figure 5a-h #518); and at least a chip, (Figure 5a-h #340), disposed onto each of the sections, (left half of the chip and the right half of the chip), of the silicon wafer, (Figure 5a-h #510), wherein the chip, (Figure 5a-h #340), includes a plurality of bonding pads, (Figure 5a-h #519), that are correspondingly connected to the pads, (Figure 5a-h #519).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,261,467 Giri et al. in view of U.S. Patent No. 5,793,105 Pace.

10. Referring to claim 16, Giri et al. in view of Pace teaches of a wafer-level package structure, (Col. 11 Lines 65-67), comprising: a silicon wafer, (Figure 1 #114 and Giri et al. is silent to the wafer being made out of silicon but is made by ceramic, but Pace does in Col. 7 Lines 1-7 teaches the wafer could be made out of silicon or ceramic and where it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the wafer out of silicon, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.), having a plurality of sections, (the terminology of a plurality of sections in a silicon wafer is being interpretated in the broadest reasonable sense because the claim does not recite any limitation that would limit it from the definition of the sections being sectioned into the left half of the chip and the right half of the chip, where Figures 5a-h shows two sections of a chip making an entire chip); a plurality of conductive blocks, (Figure 1 #122 or 121), disposed on the silicon wafer, (Figure 1 #114), and in each of the sections of the silicon wafer, (Figure 1 #114); a metal interconnect layer, (Figure 1

#126), connecting the plurality of the conductive blocks, (Figure 1 #121 or 122 is clearly in the shape of a block by simple geometry, hence the examiner is taking the broadest reasonable interpretation of the term block and where the claims and disclosure do not provide a scale where to base a narrower definition of a block), wherein the metal interconnect layer, (Figure 1 #126), comprises at least a via hole, (Figure 1 #124), and a plurality of pads, (Figure 1A #118), wherein the via hole, (Figure 1 #124), electrically connects one of the conductive blocks, (Figure 1 #121 or 122), and one of the pads, (Figure 1A #118), and wherein the pads, (Figure 1A #118), are disposed on an uppermost surface of the metal interconnect layer, (Figure 1 #126); and at least a chip, (Figure 1 Chip), disposed onto each of the sections of the silicon wafer, (Figure 1 #126), wherein the chip, (Figure 1 Chip), includes a plurality of bonding pads, (Figure 1A #118), that are correspondingly connected to the pads, (Figure 1A #118).

11. Referring to claim 17, Giri et al. in view of Pace teaches of a wafer-level package structure of claim 16, further comprising a passivation layer, (Figure 1 #112), covering each section of the wafer, (Figure 1 #126).

12. Referring to claim 18, Giri et al. in view of Pace teaches of a wafer-level package structure of claim 16, wherein the metal interconnect layer, (Figure 1 #126), further includes an oxide layer, (Figure 1 #108 and Col. 4 Lines 26 & 49-53), between the conductive blocks, (Figure 1 #121 or 122), and the pads, (Figure 1A #118), while the via hole, (Figure 1 #124), through the oxide layer, (Figure 1 #108), connects one of the conductive blocks, (Figure 1 #121 or 122), and one of the pads, (Figure 1A #118).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VAMJ
1/17/07

EVAN PERT
PRIMARY EXAMINER